How to Realize the Promise of GaN
System-Level Considerations

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Power Semiconductors are Full of Promises

- Silicon
  - Reliable
  - Decades old technology
  - Cheap!

- GaN
  - Faster!
  - Better FOMs
  - No Reverse Recovery
  - Smaller Die
  - Eventually - Cheaper?

Which of these “promises” will make a difference, and which are just marketing?

It’s the device challenges which will limit adoption - not the FoM promises
Power Converter Figures of Merit

- Cost, cost, cost
- Power Density
- Reliability
- Passing EMC, UL, Government regulations
- Secondary figures of merit:
  - Efficiency
  - Switching Frequency
What Matters in Switching Power Converters?

- Efficiency
- Power Density
- Physical System Thermal Limit

Switching Frequency

Improved Technology
Base Technology

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When does Switching Frequency Help?

- Core Loss does get better at higher frequency
- Inductors with "small" ripple get better
- "Large" ripple inductors are a mixed bag:
  - Core loss improves
  - Skin & proximity effect is worse
- Transformers are impacted more from skin and proximity loss; gains are modest

Log-Linear Plot

Ferroxcube data handbook
Hard vs. Soft Switching

Advantages of GaN: Hard Switching
- Low/zero reverse recovery enables hard-switched half bridges & new topologies
- Very fast switching speed reduces switching loss
- Lower Qoss reduces switching loss in a bridge

Advantages of GaN: Soft Switching
- Zero first-order switching loss
- Scale frequency to reduce circuit size
- Reduced Coss improves frequency scaling
- Zero Qrr allows for occasional hard-switching

Challenges using GaN: Hard Switching
- Lead inductance degrades switching performance
- Low inductance vs. thermals
- Gate drive CMTI and difficulty driving "cleanly"
- Hard-switched reliability concerns: hot carriers
- Cascode challenges: static & dynamic Si breakdown

Challenges using GaN: Soft Switching
- RMS currents increase compared with hard switching
- Rds,on the primary loss driver
- Silicon comes back into play
  - Higher parasitics hurt frequency scaling
  - Lower cost per Rds,on ➔ bigger devices
- Unmodeled high-frequency effects
Application: Server/Telecom AC/DC

Case Study: 1 kW, 12V output

Front-End PFC Stage
- Standard or 2-phase Boost PFC
- CCM Totem-Pole PFC
- Transition-Mode Totem-Pole PFC

Output DC/DC Stage
- Two-switch Forward
- Half/Full-Bridge
- Phase-Shift Full Bridge
- LLC Resonant

- 80 Plus test type
  - 80 Plus: 81% 85% 81%
  - 80 Plus Bronze: 81% 85% 81%
  - 80 Plus Silver: 85% 89% 85%
  - 80 Plus Gold: 88% 92% 88%
  - 80 Plus Platinum: 90% 94% 91%
  - 80 Plus Titanium: 90% 94% 96% 91%
GaN in Standard Boost PFC Converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Silicon Device</th>
<th>GaN Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ds, on}$ (typ) @ 25°C</td>
<td>62 mΩ</td>
<td>67 mΩ</td>
</tr>
<tr>
<td>$R_{ds, on}$ (typ) @ 100°C</td>
<td>105 mΩ</td>
<td>120 mΩ</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>64 nC</td>
<td>4.4 nC</td>
</tr>
<tr>
<td>$E_{oss}$</td>
<td>8 µJ</td>
<td>5.3 µJ</td>
</tr>
</tbody>
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- **230V**: GaN efficiency slightly higher than Silicon Superjunction at high output powers.
- **115V**: Silicon Superjunction shows a better efficiency curve compared to GaN at lower output powers.

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Boost Converter - Loss Breakdown

Why the small difference?

- Gate loss is negligible in both cases
- Switching against SiC diode; no reverse recovery
- Eoss is considered, not Qoss
- SiC diodes and Superjunction MOSFETs optimized for PFC boost!
Choose Topology to Take Advantage of GaN!

- Good in all hard-switched half-bridge topologies
- Totem-Pole PFC eliminates all diode drops
- Reduce BOM count, solution size
CCM Totem-Pole PFC Frequency Scaling

65% Less Core Volume

Power Loss Components

- Core
- Winding
- FET Ron
- Diode Leg
- Switching
- Coss
- Gate

Efficiency [%]

Output Power [W]

Loss [W]

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**Soft switching will allow for frequency scaling**

- Shrink inductance to allow for inductor current commutation on both edges
- Frequency will vary over line cycle and with line and load
- RMS currents will increase -> **need to increase FET size to 45 mΩ**
Frequency Scaling of TM Totem-Pole PFC

Loss Breakdown:
- Diode Leg: 21.8%
- Core: 39.1%
- FET Ron: 25.4%
- Winding: 13.6%
- Gate: 0.1%

Mid-Load Efficiency:
- Efficiency limited by core material availability

Core Volume [mm³]:
- 78% Less Core Volume

Average Switching Frequency [kHz]:

Efficiency:
- 99%
- 98%
- 97%
- 96%
- 95%
- 94%
- 93%
- 92%
- 91%
- 90%
- 89%
- 88%
- 87%
- 86%
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- 4%
- 3%
- 2%
- 1%
- 0%
(R)evolution of Power Design

Traditional Power Design

Silicon Power Switches
- Large Parasitics - especially Qrr

Hard-Switched “Textbook” Topologies
- Fixed frequency and hard switching

PWM Power Controllers
- Fixed frequency, PWM, analog or PID-digital
- Sometimes current-mode control

Traditional Analysis
- SPICE, SIMPLIS, PSIM, Matlab, Excel...
- Textbook segmented analysis and design

Tomorrow’s Power Design

Wide Bandgap Power Switches
- Nearly Ideal - no/low Qrr
- Much Faster

(Quasi-)Resonant & ZVS Topologies
- Variable frequency, soft switching
- Little/no switching loss allows for fast frequencies

Flexible Hybrid Power Controllers
- Programmable, digital control with flexible analog
- Flexible, fast analog triggers to support ZVS/ZCS

Modern Multi-Disciplinary Analysis
- Full analysis of ZVS/Resonant topologies
- Concurrently create topology, control & magnetics
Need for Semiconductor Packaging

Low Inductance

- Low inductance to reduce ringing, switching loss and EMI noise
- Large copper area and thickness to spread heat
  - TIM is often the limiting factor
- Package with heat sink satisfies creepage and clearance
- Incredibly robust and reliable!

Good Thermals

Low Inductance & Good Thermals?

- Low inductance to reduce ringing, switching loss and EMI noise
- Large copper area and thickness to spread heat
  - TIM is often the limiting factor
- Package with heat sink satisfies creepage and clearance
- Incredibly robust and reliable!
Need for Semiconductor Support

**Gate Drivers**
- Fast, ≤ 10ns prop times for accurate ZVS reactions
- Highly integrated: reduce auxiliary IC count
- Accurate Vgs regulation for reliability
- High CMTI (dv/dt) ≥ 100 V/ns
- Low inductance package

**Controllers**
- Programmable digital controllers for flexibility and communications
- Analog or HW digital inner loops for speed: support ≥ 1MHz
- Analog “trip points” triggered by ZVS events; flexible handling
- Flexible, powerful design environment
Conclusions

- GaN (& SiC) is motivated by superior FOMs but its really circuit performance that matters
- End goal: *Power density* (not efficiency or switching frequency)
- Circuit performance (vs. Silicon) depends on topology and control
- Soft-switched topologies still offer advantages in power density (via frequency scaling)
- Ecosystem content: Semiconductor drivers and controllers are needed to make soft-switched topologies widespread (not just GaN!)
- Cost: While GaN is coming down in price – the highly-integrated silicon content needs to follow to keep system cost low!